WHAT IS CLAIMED IS:

1. A method for manufacturing a ferroelectric capacitor, comprising:

forming a first electrode layer;

forming a ferroelectric dielectric layer over the first electrode layer;

planarizing the ferroelectric dielectric layer to form a planarized ferroelectric dielectric layer; and

forming a second electrode layer over the planarized ferroelectric dielectric layer.

2. The method as recited in Claim 1 wherein planarizing the ferroelectric dielectric layer includes planarizing the ferroelectric dielectric layer using a chemical mechanical polishing process until it is substantially planar.

3. The method as recited in Claim 2 wherein the substantially planar ferroelectric dielectric layer has an average surface roughness of less than about 1 nm.

4. The method as recited in Claim 3 wherein the substantially planar ferroelectric dielectric layer has an average surface roughness of less than about 0.5 nm.

5. The method as recited in Claim 1 wherein the ferroelectric dielectric layer comprises lead zirconate titanate (PZT) or strontium bismuth tantalate (SBT).

6. The method as recited in Claim 1 further including cleaning the planarized ferroelectric dielectric layer prior to forming the second electrode layer.

7. The method as recited in Claim 1 further including forming a first protective layer between the first electrode layer and a conductive plug and forming a second protective layer over the second electrode layer.

8. The method as recited in Claim 7 further including planarizing at least a portion of the second electrode layer to form a planarized second electrode layer prior to forming the second protective layer.

9. The method as recited in Claim 8 further including cleaning the planarized second electrode layer prior to forming the second protective layer.

10. The method as recited in Claim 1 further including planarizing at least a portion of the first electrode layer to form

a planarized first electrode layer prior to forming the ferroelectric dielectric layer.

11. The method as recited in Claim 10 further including cleaning the planarized first electrode layer prior to forming the ferroelectric dielectric layer.

12. The method as recited in Claim 1 wherein the ferroelectric dielectric layer has a thickness ranging from about 150 nm to about 60 nm and the planarized ferroelectric dielectric layer has a thickness ranging from about 100 nm to about 20 nm.

13. The method as recited in Claim 1 further including patterning the first electrode layer, the ferroelectric dielectric layer, and the second electrode layer to form a patterned ferroelectric capacitor.

14. A ferroelectric capacitor, comprising:

a first electrode layer;

a substantially planar ferroelectric dielectric layer located over the first electrode layer, wherein the substantially planar ferroelectric dielectric layer has an average surface roughness of less than about 4 nm; and

a second electrode layer located over the substantially planar ferroelectric dielectric layer.

15. The ferroelectric capacitor as recited in Claim 14 wherein the substantially planar ferroelectric dielectric layer has an average surface roughness of less than about 1 nm.

16. The ferroelectric capacitor as recited in Claim 14 wherein the substantially planar ferroelectric dielectric layer comprises lead zirconate titanate (PZT) or strontium bismuth tantalate (SBT).

17. A method for manufacturing a ferroelectric random access memory (FeRAM) device, comprising:

forming a transistor having source/drain regions over a semiconductor substrate;

forming an interlevel dielectric layer over the transistor, the interlevel dielectric layer having a conductive plug therein contacting at least one of the source/drain regions; and

forming a ferroelectric capacitor over the interlevel dielectric layer and contacting the conductive plug, including;

forming a first electrode layer over the conductive plug;

forming a ferroelectric dielectric layer over the first electrode layer;

planarizing the ferroelectric dielectric layer to form a planarized ferroelectric dielectric layer; and

forming a second electrode layer over the planarized ferroelectric dielectric layer.

18. The method as recited in Claim 17 wherein planarizing the ferroelectric dielectric layer includes planarizing the ferroelectric dielectric layer using a chemical mechanical polishing process until it is substantially planar.

19. The method as recited in Claim 18 wherein the substantially planar ferroelectric dielectric layer has an average

surface roughness of less than about 1 nm.

20. The method as recited in Claim 19 wherein the substantially planar ferroelectric dielectric layer has an average surface roughness of less than about 0.5 nm.

21. The method as recited in Claim 17 wherein the ferroelectric dielectric layer comprises lead zirconate titanate (PZT) or strontium bismuth tantalate (SBT).

22. The method as recited in Claim 17 further including cleaning the planarized ferroelectric dielectric layer prior to forming the second electrode layer.

23. The method as recited in Claim 17 further including forming a first protective layer between the first electrode layer and a conductive plug and forming a second protective layer over the second electrode layer.

24. The method as recited in Claim 23 further including planarizing at least a portion of the second electrode layer to form a planarized second electrode layer prior to forming the second protective layer.

25. The method as recited in Claim 24 further including cleaning the planarized second electrode layer prior to forming the second protective layer.

26. The method as recited in Claim 17 further including planarizing at least a portion of the first electrode layer to form a planarized first electrode layer prior to forming the ferroelectric dielectric layer.

27. The method as recited in Claim 26 further including cleaning the planarized first electrode layer prior to forming the ferroelectric dielectric layer.

28. The method as recited in Claim 17 wherein the ferroelectric dielectric layer has a thickness ranging from about 150 nm to about 60 nm and the planarized ferroelectric dielectric layer has a thickness ranging from about 100 nm to about 20 nm.

29. The method as recited in Claim 17 further including patterning the first electrode layer, the ferroelectric dielectric layer, and the second electrode layer to form a patterned ferroelectric capacitor.

30. A method for manufacturing a ferroelectric capacitor, comprising:

forming a first electrode layer;

forming a ferroelectric dielectric layer over the first electrode layer; and

forming a second electrode layer over the planarized ferroelectric dielectric layer, wherein at least one of the first electrode layer, ferroelectric dielectric layer or second electrode layer is planarizing to form a planarized first electrode layer, planarized ferroelectric dielectric layer or planarized second electrode layer, respectively.

31. The method as recited in Claim 30 wherein the ferroelectric dielectric layer is planarized and cleaned prior to forming the second electrode layer.

32. The method as recited in Claim 30 wherein the second electrode layer is planarized and cleaned prior to forming an additional layer thereon.